We claim:

1. A circuit comprising:

an on-die weight generator circuit to provide an at least one weighted test data bit stream for an on-die scan chain wherein the weight of a test data bit of each of said data bit streams depends upon a corresponding data field downloaded to the weight generator circuit of a data set;

a memory to store the data set; and

a data download circuit to download each data field of the data set from the memory to the weight generator circuit in synchronization with the weight generator circuit providing the corresponding test data bit to each said test data bit stream.

2. The circuit defined in claim 1 wherein the weight generator circuit includes a switch to generate each weighted test data bit, the switch having an input of a plural number of differently weighted bit stream and a control signal of the corresponding data field.

3. The circuit defined in claim 1 wherein the memory is an on-die memory.

4. The circuit defined in claim 1 wherein the data download circuit is an on-die circuit

5. The circuit defined in claim 1 wherein

the memory further is to store an at least one other data set; and

the data download circuit is to download each data field of each of the data sets in synchronization with the weight generator circuit providing the corresponding test data bit to each said test data bit stream for each data set.

6. The circuit defined in claim 1 wherein the data download circuit includes:

a control circuit to read each data field of the data set from the memory to a buffer system, and

the buffer system to output each data field from the data download circuit to the weight generator circuit.

7. The circuit defined in claim 6 wherein the buffer is to output the first data to the weight generator in response to a signal from the control circuit.

8. The circuit defined in claim 1 wherein each data field consists of a first range of bits, and the data download circuit includes:

a control circuit to read a data of the data set from the memory at a second range of bits at a second time periods to a buffer circuit, and

the buffer circuit to output each data field from the data download circuit to the weight generator circuit at a second time periods.

9. The circuit defined in claim 8 wherein the buffer is to output the first data to the weight generator in response to a signal from the control circuit.

10. A method comprising:

providing a weighted test data bit stream from a weight generating unit to a scan chain disposed on an integrated circuit die wherein the weight of a bit of the bit stream depends upon a corresponding data field downloaded to the weight generating unit of a data set;

storing at least one data set in a memory unit; and

downloading to the weight generating unit the corresponding data field from the memory in synchronization with the weight generating unit providing a corresponding bit of the bit stream.

11. The method defined in claim 10 wherein the weight generating unit is disposed on the integrated circuit die.

12. The method defined in claim 10 wherein the memory unit is disposed on the integrated circuit die.

13. The method defined in claim 10 wherein the weight generating unit includes a switch of the type that outputs one of a plurality of inputs depending upon a content of a control signal, and the providing includes inputting to the switch a plurality of differently weighed bit streams wherein the control signal substantially consists of the corresponding data field.

14. The method defined in claim 10 wherein the downloading includes reading a portion of at least one of the data sets from the memory at a rate of a first number of bits at a first set of times, storing the read portion in a buffering circuit, and downloading from the buffering circuit a data field at a second set of times, the second set of times being in synchronization with the data bit stream rate such that the weight of a bit of the bit stream depends upon the corresponding data field.

15. A circuit comprising:

an at least one weight generator circuit, each said weight generator circuit to provide a distinct test data bit stream to a distinct integrated circuit test scan chain, wherein each said weight generator circuit is to determine a bit of a provided test data bit stream weight depending upon a corresponding stored control signal provided to the weight generator circuit from a control signal generating unit disposed on the die of the integrated circuit.

16. The circuit defined in claim 15 wherein the control generating circuit includes both a memory unit and a control circuit to download each of the stored control signal from the memory unit to the weight generator circuit in synchronization with the weight generator circuit determining a bit.

17. The circuit defined in claim 15 wherein the memory unit is a memory unit of the integrated circuit.